Work Package 6: Real-time simulator

Project #671662 funded by European Commission under program H2020-EU.1.2.2 coordinated in H2020-FETHPC-2014

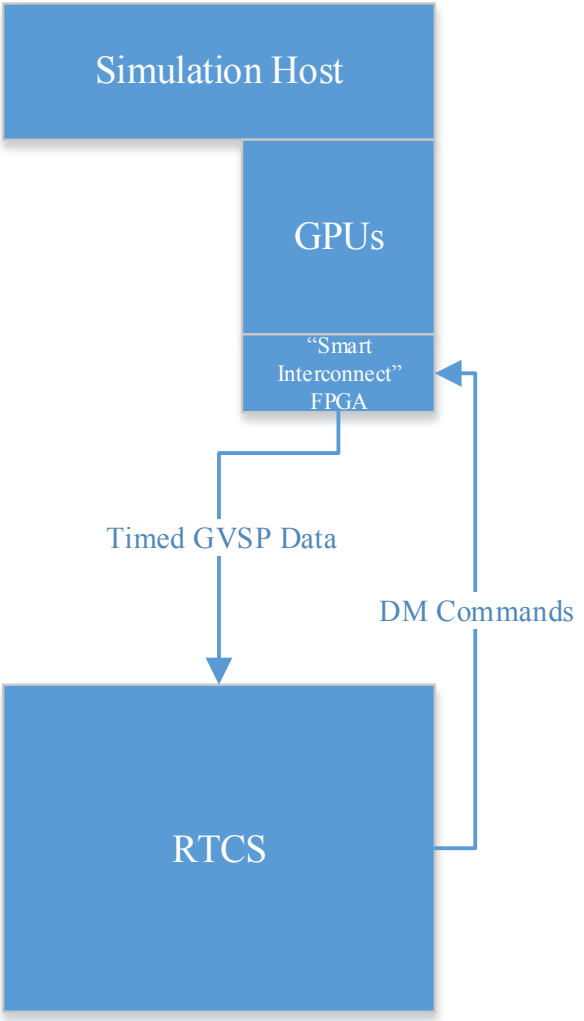
High Level Design

- 2 Distinct Modes:

- Simulation Rate Mode
  - Runs as fast as end-to-end simulation
  - Feedback from RTC into simulation
- “Fast Mode”
  - Runs at real-time rate

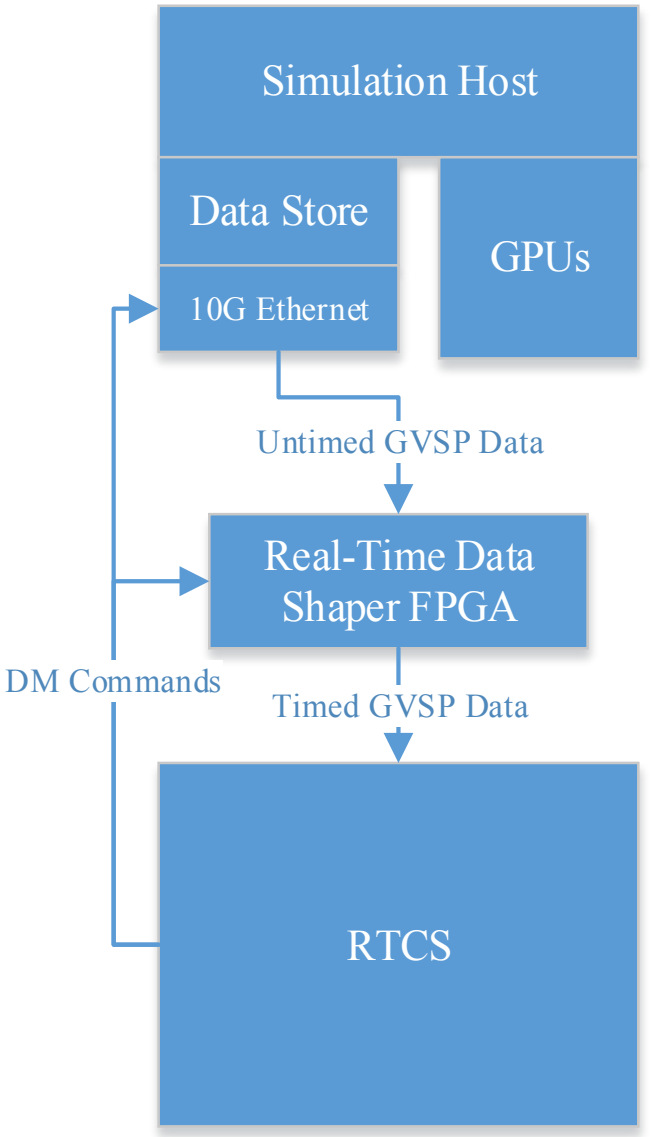
Simulation Rate Mode

- Developed primarily at LESIA
- COMPASS GPU accelerated end to end simulation
- Outputs data directly to Ethernet as GVSP
- Accepts DM commands to close simulated AO loop

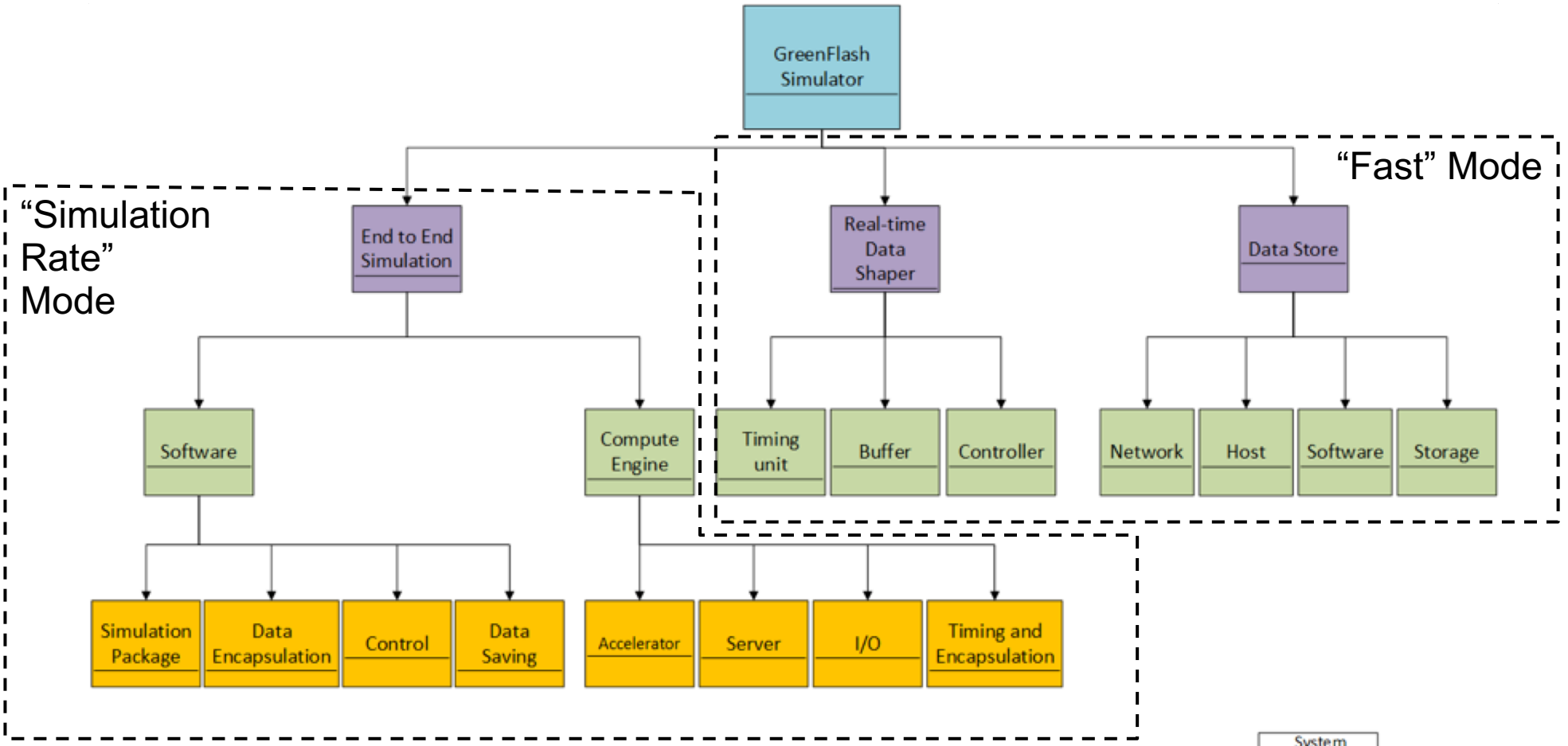


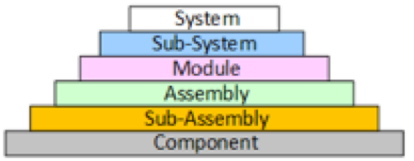
Fast Mode

- Developed primarily at Durham
- Provides saved WFS data at on-sky rates (up to 1000 Hz)
- All data sent deterministically over GVSP
- Timing provided by FPGA to give latency measurements



Product Breakdown





Data Store

- Stores WFS detector data to be quickly sent as if from a camera

- Requirements:
  - ~500GB (60s of 6 WFSs, 800x800 pixels @ 1kHz
  - Read speed of >60Gbit/s (~7.5GB/s)

- No one hard drive on the market meets these requirements
  - Fastest consumer SSD is Samsung 960 (read speed ~3.2GB/s)

- Can combine multiple SSDs as RAID for extra speed

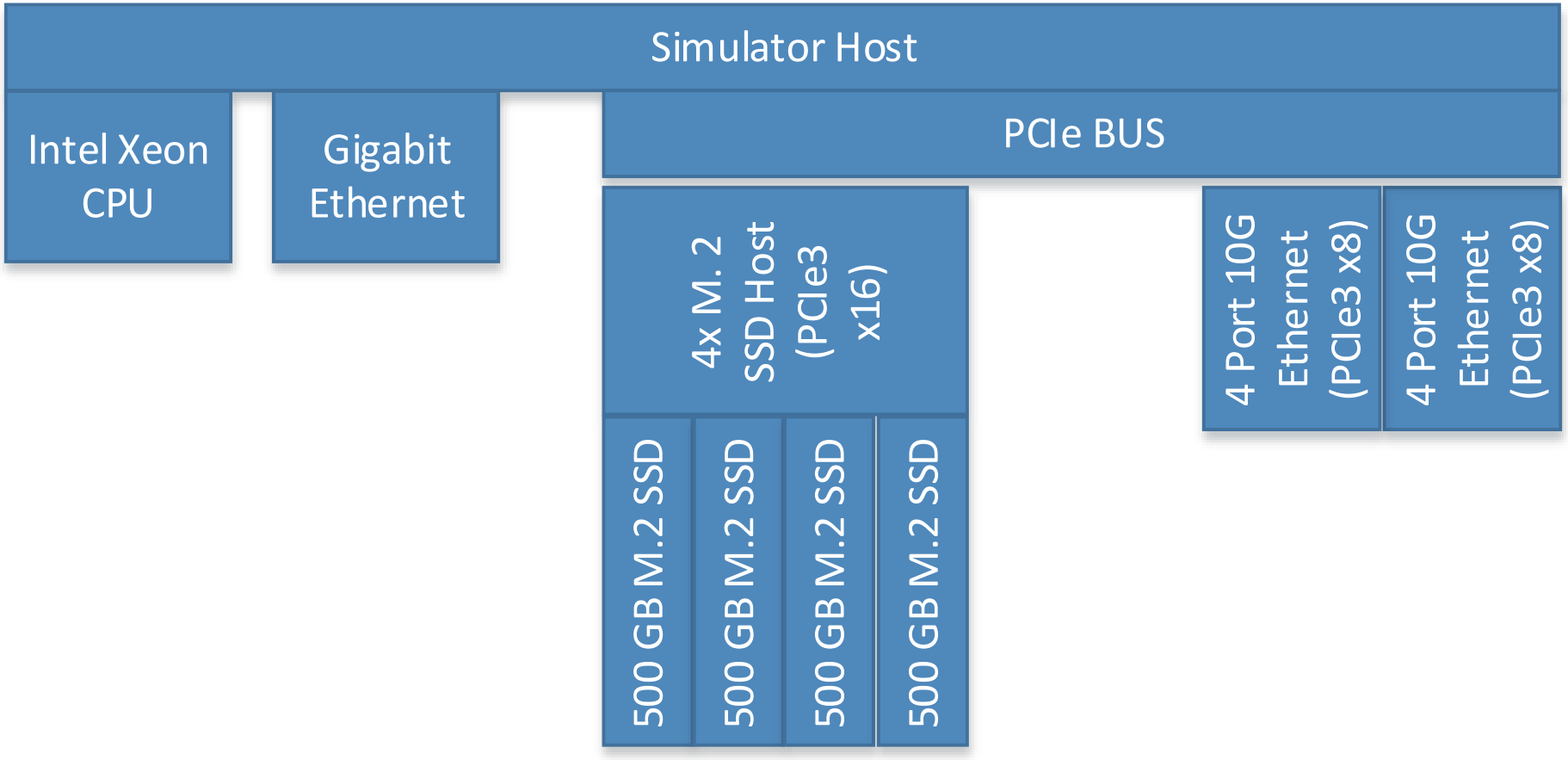
l'Observatoire de Paris Durham University MICROGATE PLDA

Data Store

- Amfeltec “SKU-086-34 SQUID PCIe Carrier Board” holds 4 M.2 SSDs

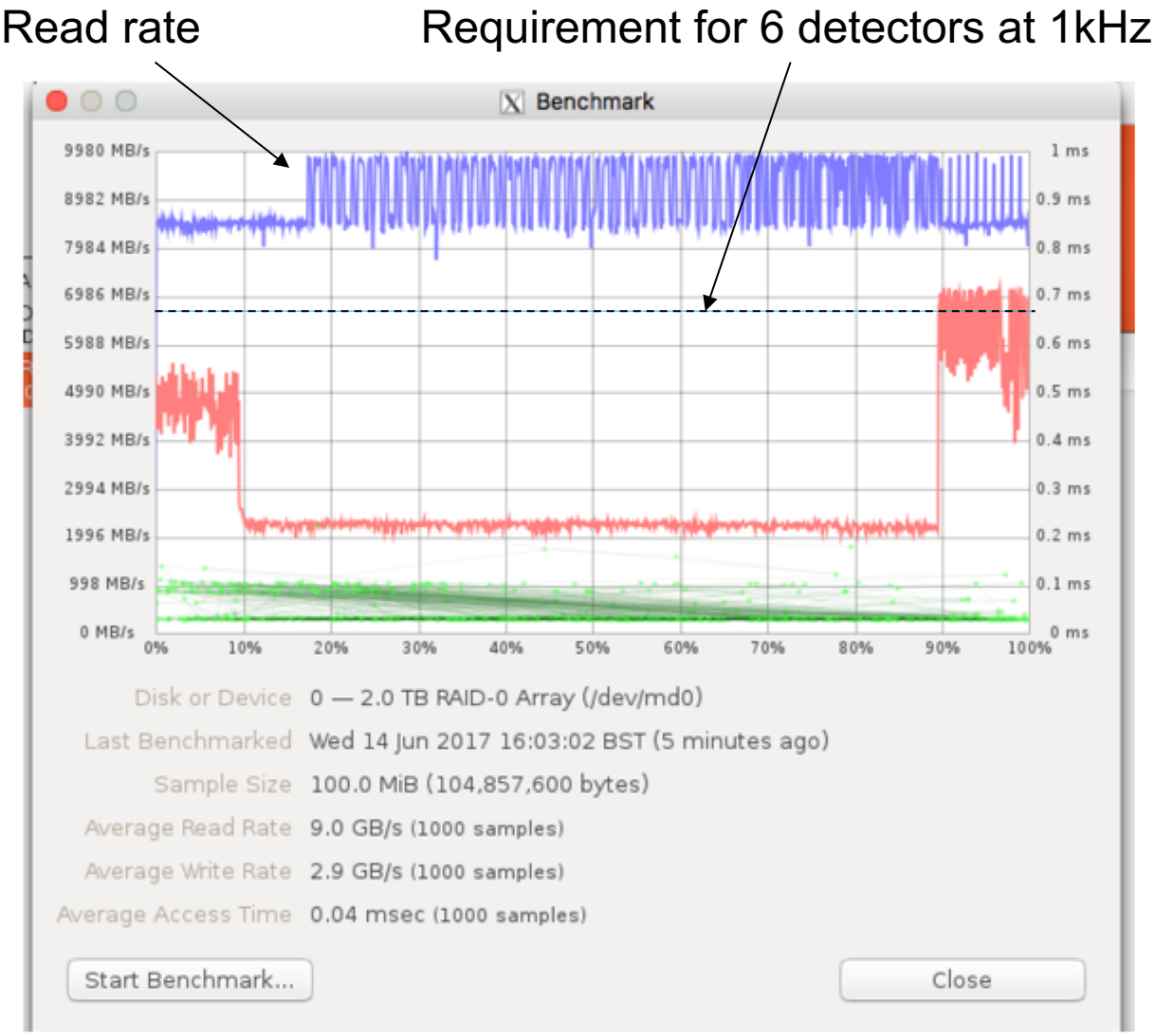
- Theoretically operate at up to ~12 GB/s with 4 SSDs in RAID 0 array

Data Store


Simulator Host
Intel Xeon CPU
Gigabit Ethernet
PCIe BUS
4x M. 2 SSD Host (PCIe3 x16)
500 GB M.2 SSD
500 GB M.2 SSD
500 GB M.2 SSD
500 GB M.2 SSD
4 Port 10G Ethernet (PCIe3 x8)
4 Port 10G Ethernet (PCIe3 x8)

Data Store, Initial tests

- Received and integrated
- Read performance in RAID 0 array meets requirements.
- Dependent on file size and array parameters
- Benchmarks show 8 – 12 GB/s read speeds



Data Store - Software

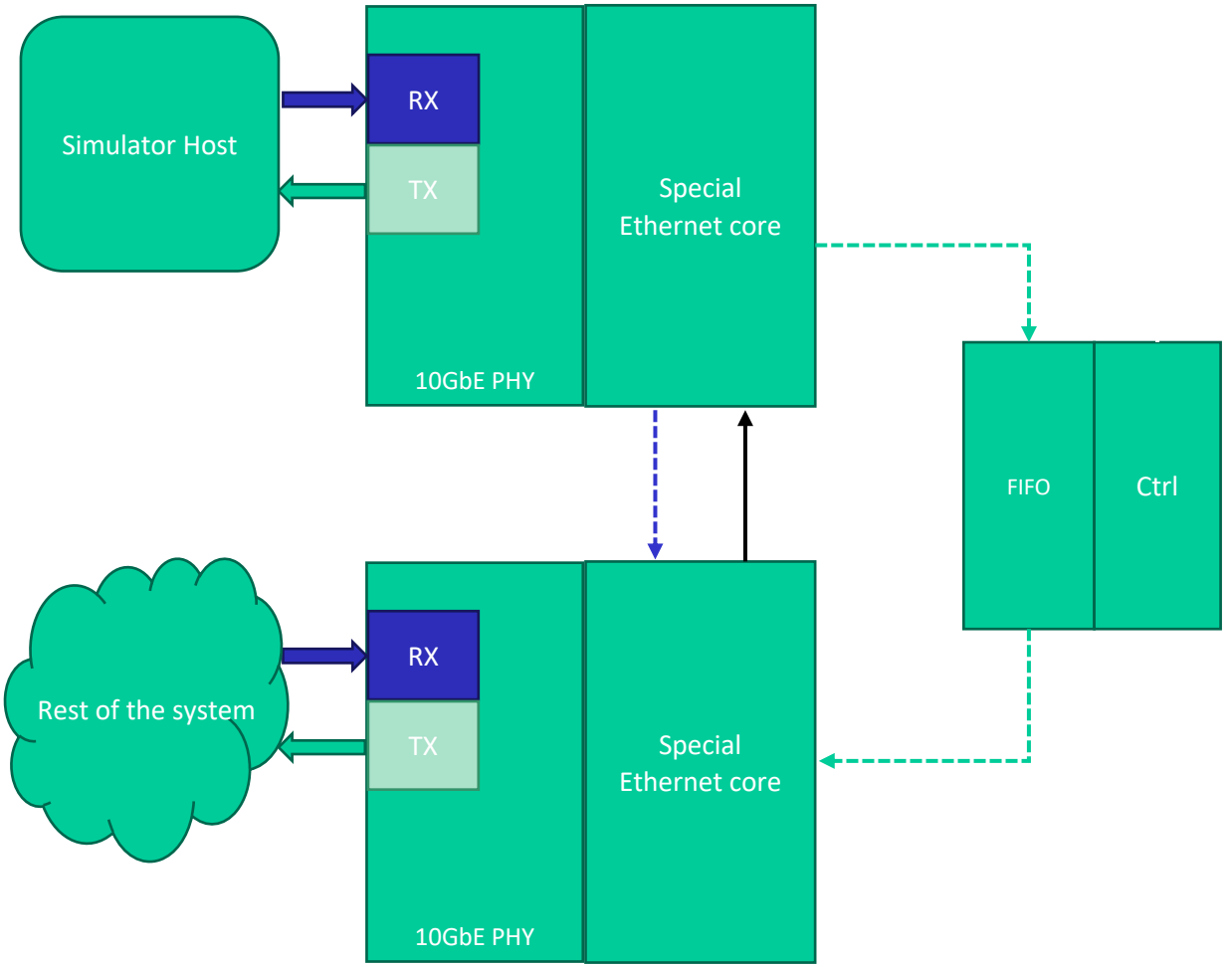
- Must send data using GVSP protocol

- Use existing “Fake Camera” module from open source “Aravis” GigeVision Library
  - Sends data from an arbitrary source using GVSP
  - Required patches to operate with 16bit data
  - Written basic python interface to load FITS file

Real-Time Data Shaper

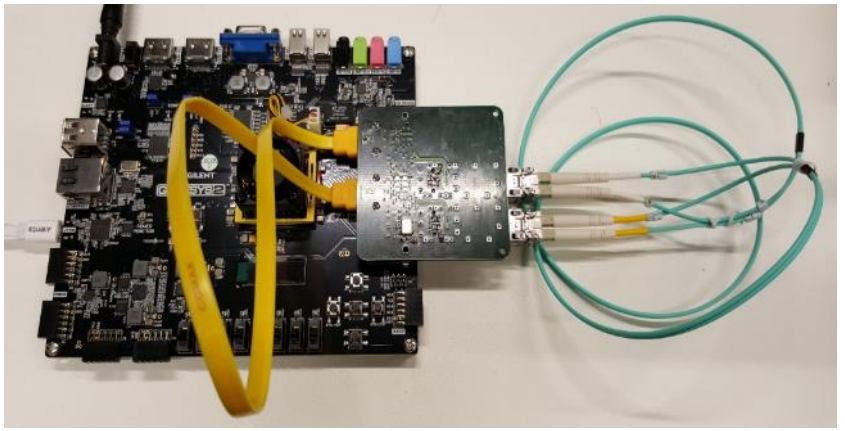
- “Shapes” the detector data such that frames are sent deterministically to the RTC
- Requirements
  - Network “Transparent” – simulator can be operated with or without data shaper
  - Can accurately time sending of each frame
  - Can receive DM commands to measure latency of RTC

Data Shaper Design

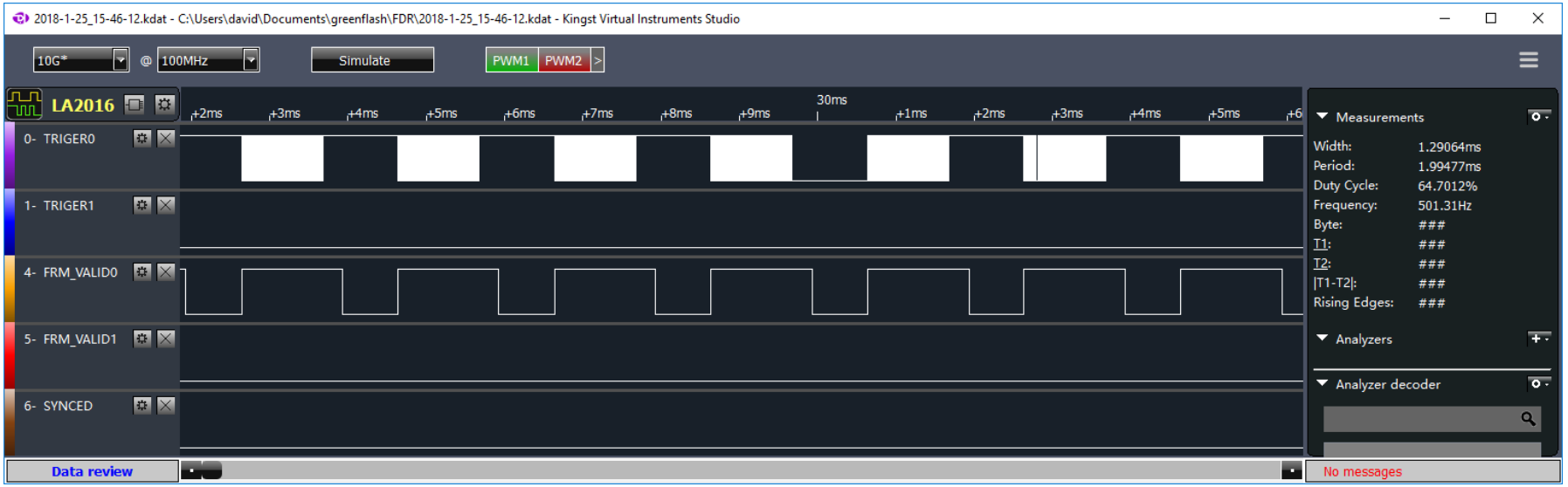


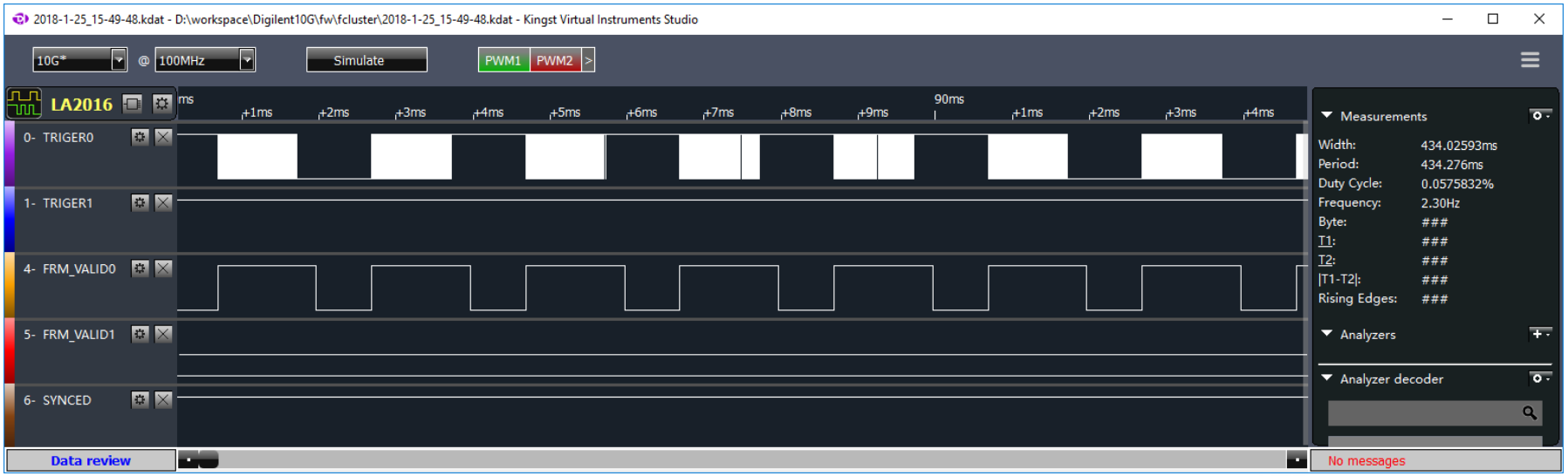
Real-time Data Shaper

- Based on Digilent Genesys2 board with in-house built 10GbE SFP+ adaptor
- 10GbE core implemented and tested
- Implemented Ethernet “Pass-through”
- Implemented UDP packet buffer-and-forward
- Built-in Ethernet packet to TTL conversion for UDP latency and jittering measurements

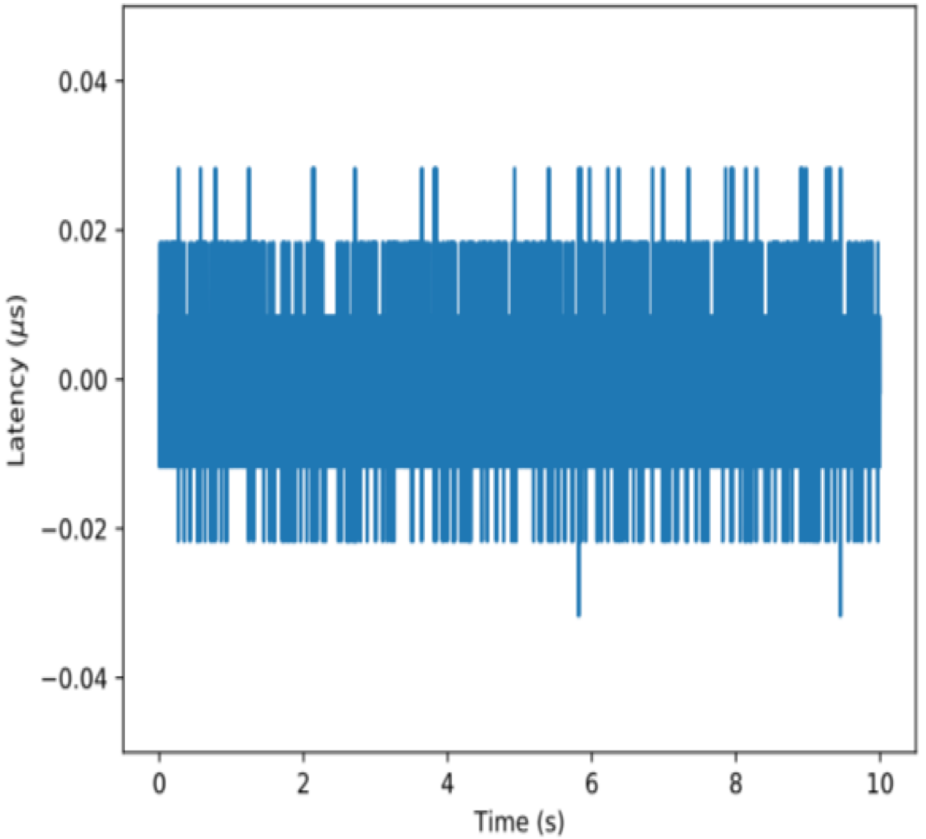


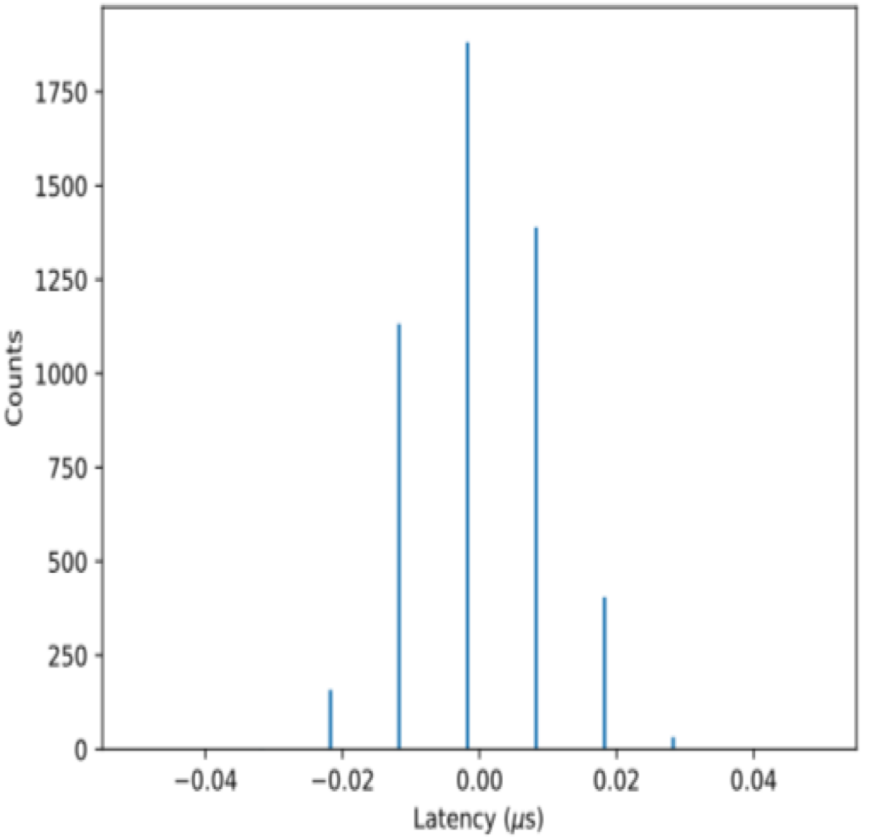
Real-time Data Shaper Multi-Channel





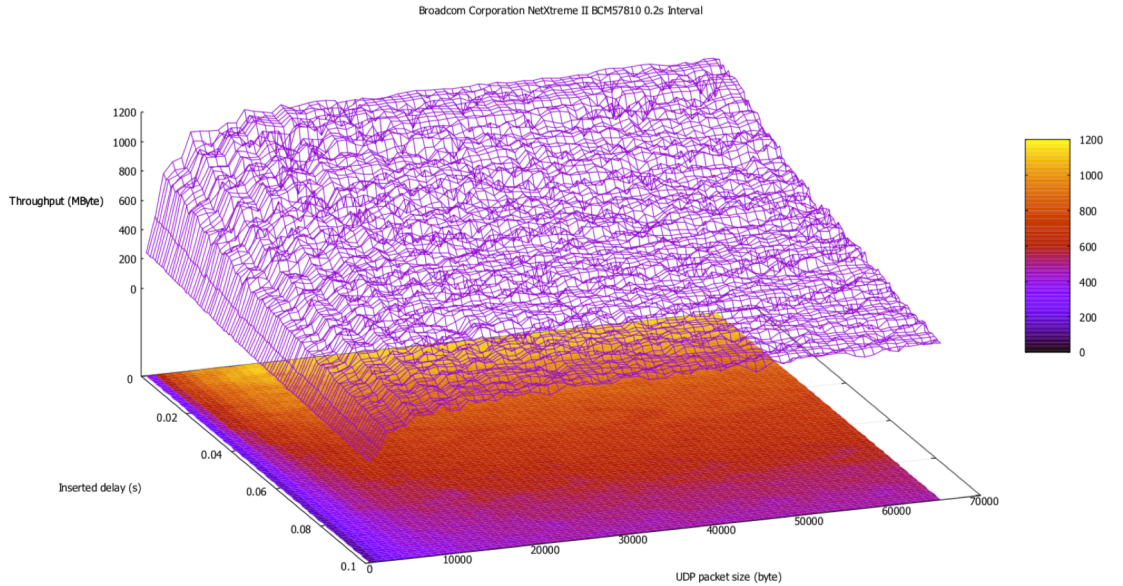
Latency and Jitter

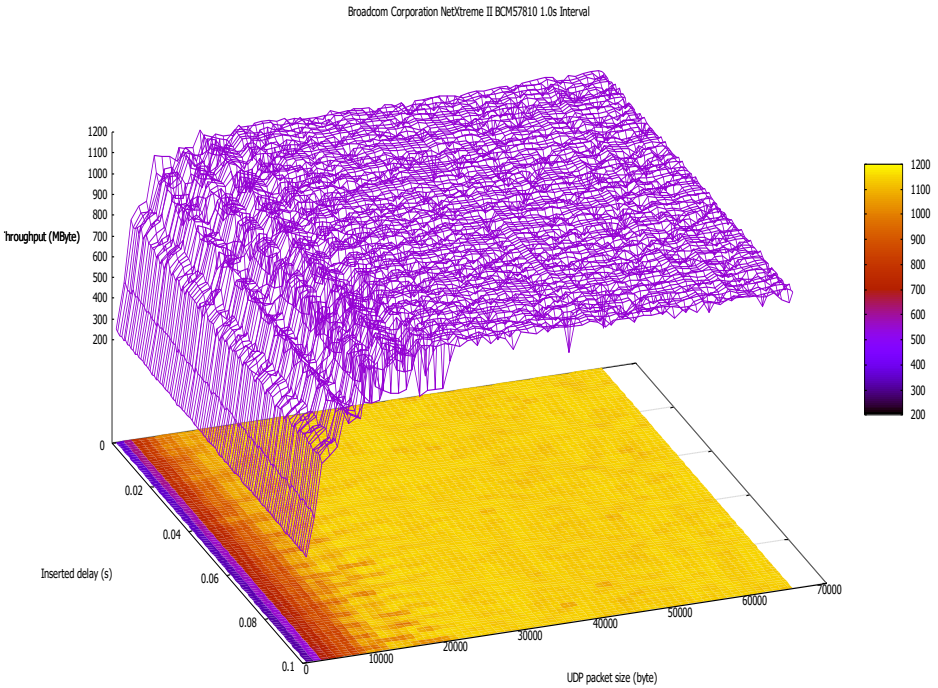




10GbE Benchmark

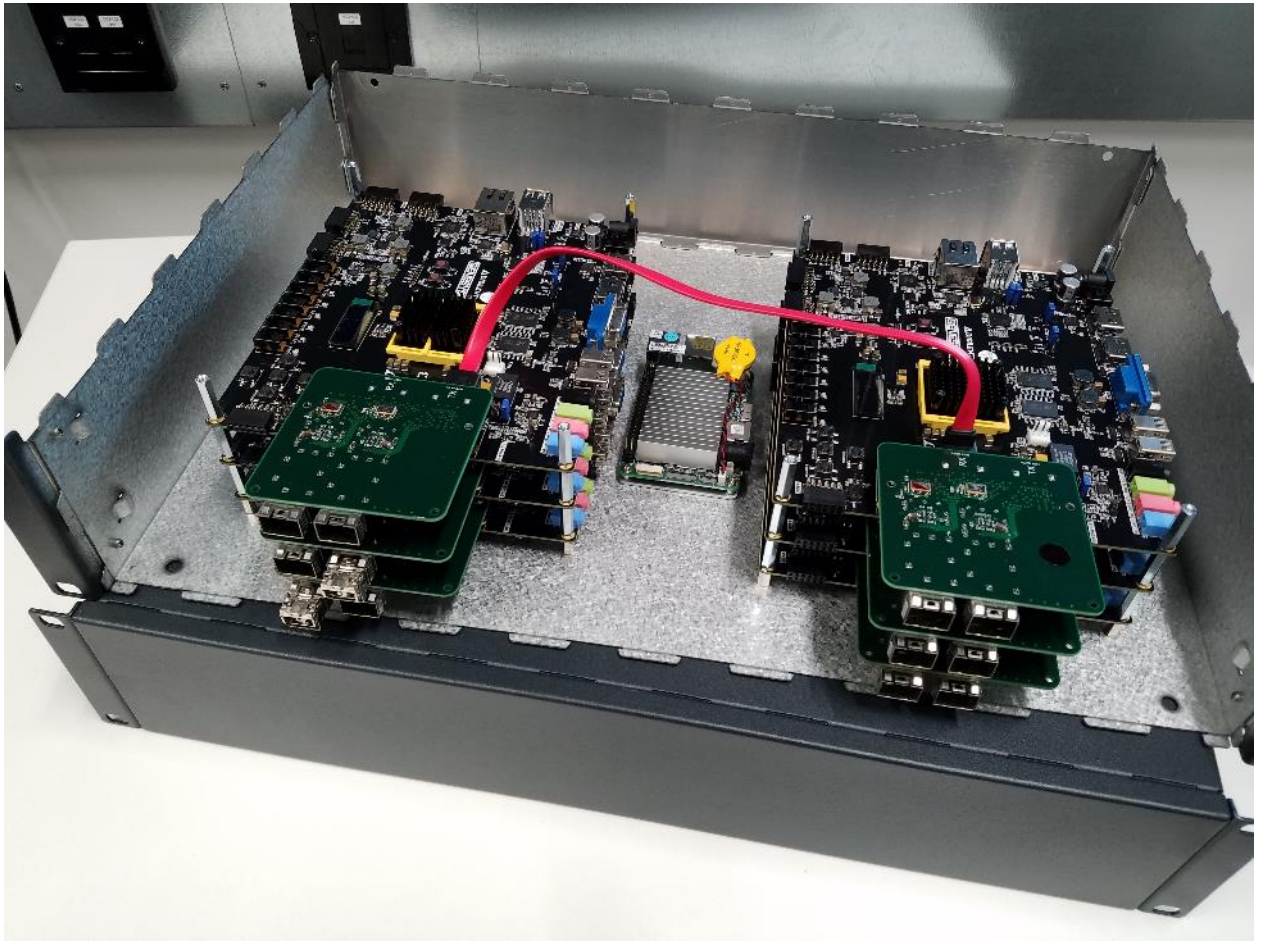
- Tested with different UDP packet size
- To simulate the interruption
  - Tested with regular input latency interruptions (of increasing delay value)
  - Tested with random latency interruptions every 1s





RTDS

- Same hardware reused as data shaper and acceleration cluister by different FPGA firmware configuration
- 6 FPGA cards in a 2U chassis
- Multiple 10GbE SPF+ sockets
- Internal interconnection using SATA sockets
- Tiny PC inside for FPGA configuration at run-time as well as FPGA cluster high-level interface



Simulator “Real-time rate” Status

- Can emulate GVSP camera, sending arbitrary saved data from memory mapped FITS file
- Received and integrating fast data store
- Prototype of the RT data shaper achieved low frame jittering about 0.2~0.3us